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*D2*  
*concl*

wherein said filler material has an upper surface which is unpolished and co-planar with a upper surface of said substrate.

*SUB E3*

23. (Thrice Amended) A semiconductor substrate having a planarized structure formed according to a method comprising:

- forming a pad on a surface of said substrate;
- forming at least one trench in said substrate;
- applying a seamless filler material by high density plasma method in said at least one trench and on said pad, said filler material filling at least a portion of said at least one trench;
- selectively removing said filler material on said pad so as to separate said filler material in said at least one trench and said filler material on said surface by an exposed area of said pad, and
- removing said filler material on said pad while allowing said filler material in said at least a portion of said at least one trench to remain,

wherein said filler material has an upper surface which is unpolished and co-planar with a upper surface of said substrate.

*D3*

*D4* *SUB G17*

25. (Amended) The semiconductor substrate according to claim 8, wherein said at least one trench comprises at least one wide trench and at least one narrow trench.

*SUB E4*

29. (Amended) The semiconductor substrate according to claim 8, wherein said surface of said filler material and said surface of said substrate are planarized without reactive ion etching.

*D5*

Please add the following new claims:

*SUB E5*

- - 31. The semiconductor substrate according to claim 8, wherein said surface of said filler material and said surface of said substrate are planarized without chemical mechanical polishing.

*D6* *E*

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32. The semiconductor substrate according to claim 8, wherein said surface of said filler material is substantially scratch-free.

*D6*  
*concl*  
33. The semiconductor substrate according to claim 8, wherein said surface of said substrate comprises implanted dopants. *E*

34. The semiconductor substrate according to claim 8, further comprising:  
a thin oxide layer grown on said upper surface of said substrate.

35. The semiconductor substrate according to claim 8, wherein said surface of said filler material is free of chatter marks. - -

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